NEW BRIEF DESCRIPTION OF DRAWINGS FROM PAGE 7,

LINE 6 TO PAGE 8, LINE 15:

Brief Description of the Drawings

The invention will now be described in greater detail with specific reference to the appended drawings wherein:

Fig. 1 shows a typical hysteresis I-V switching loop for a PZT ferroelectric film and operating characteristics therefor;

Fig. 2A shows a first alternative prior art implementation of a planar on-chip capacitor;

Fig. 2B shows a second alternative prior art implementations of a deep trench on-chip capacitor;

Figs. 3A through 3C provide schematic views of lateral decoupling capacitor in accordance with the present invention;

Figs. 4A through 4G provide side cutaway views of a process flow for fabricating the structure of Fig. 3C;

Fig. 5 provides a side perspective view of an alternative vertical embodiment of a decoupling capacitor in accordance with the present invention;

Fig. 6 provides a top view of a semiconductor structure in accordance with the present invention, which includes lateral decoupling capacitors both between adjacent interconnect lines on a level and vertical decoupling capacitors between interconnect levels;

Figs. 7A through 7F provide illustration of a process flow for fabricating the on-chip decoupling capacitor of Fig. 3A;

Figs. 8A through 8K provide illustration of a process flow for fabricating the on-chip decoupling capacitor of Fig. 5; and

Fig. 9 provides a side perspective view of an alternative vertical embodiment of a decoupling capacitor with multiple successive layers in accordance with the present invention.

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Fig. 9 provides a side perspective view of an alternative embodiment of a high-k decoupling capacitor in accordance with the present invention wherein the high-k material is vertically disposed between metal lines on the semiconductor substrate. The materials which are suitable for the lateral embodiment would

necessarily be appropriate for the vertical embodiment and will not be repeated herein. The vertical capacitor is formed of metal line 905, metal line 915 and high-k material 919. The metal line 905 is formed in dielectric layer 902 on substrate 901. A diffusion barrier layer 927 is disposed between the metal line 905 and the high-k material 919. In addition, a diffusion barrier layer 927 is needed to isolate the high-k material from the underlying metal 905. Further, a conducting metal liner 917 is disposed in layer 912 to ensure adhesion of the metal stud 915. Metal stud 915 is formed in dielectric layer 912 and provides an interconnection between the underlying metal line 903 and the overlying metal. Next, a successive structure formed in layers 922 and 932 is disposed above the structure. Metal lines 923 and 925 are formed in dielectric layer 922 above the layer comprising 912, 917, 915, 919 and 927. A diffusion barrier layer 967 is disposed between the metal line 925 and the high-k material 969. In addition, a diffusion barrier layer 977 is needed to isolate the high-k material 979 from the underlying metal 925. Further, a conducting metal liner 987 is disposed in layer 932 to ensure adhesion of the metal stud 985. Metal stud 985 is formed in dielectric layer 932 and

provides an interconnection between the underlying metal line 923 and the overlying metal 985. Another diffusion barrier layer 937 is disposed and patterned on the surface of the structure prior to depositing metal line 933.

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361/ 303 - 306.3
311 - 313
306.1

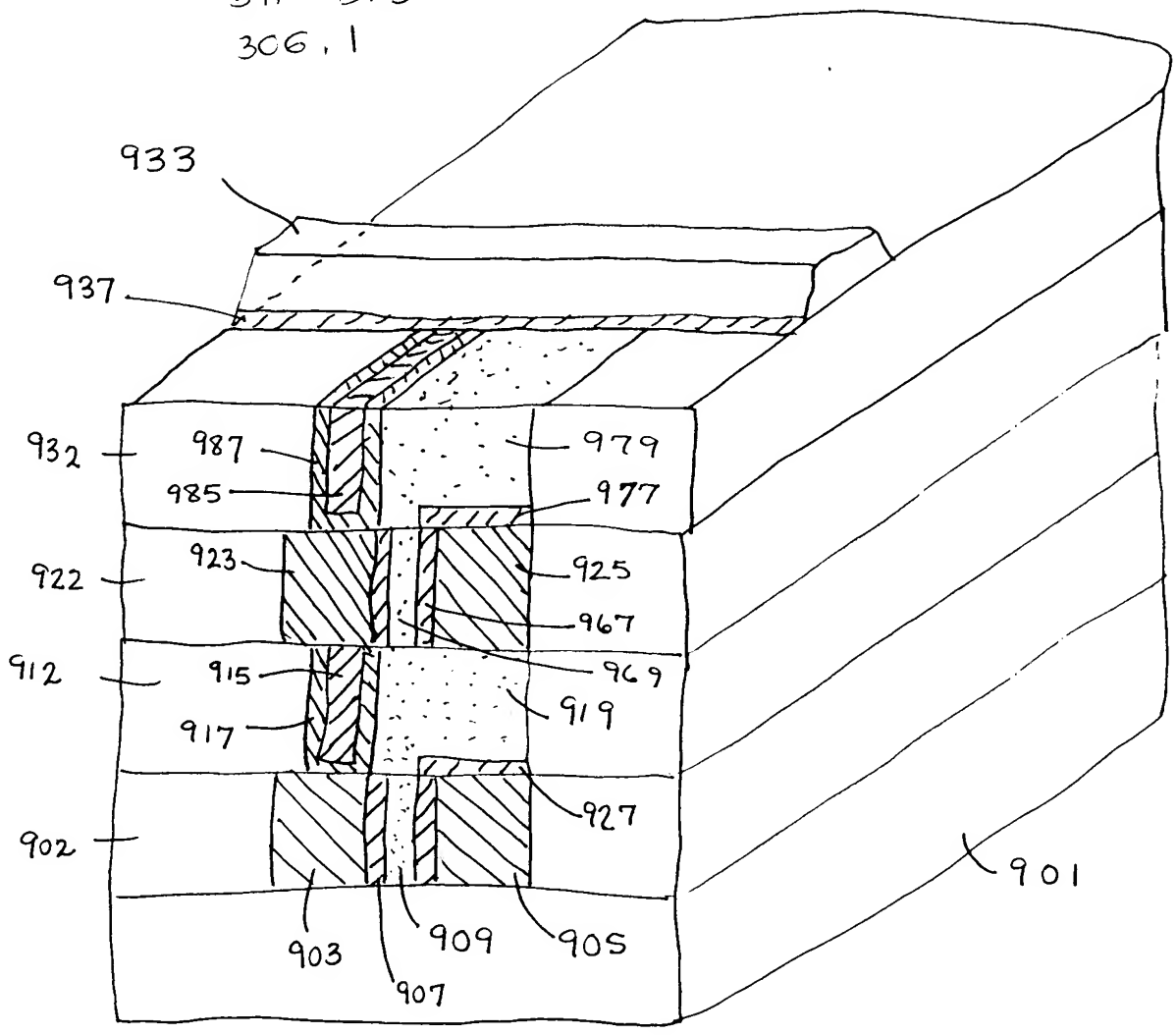

FIG. 9

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